REMARKS/ARGUMENTS

Claims 1-4 and 8 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Ichikawa in view of Coats, Jr. (herein after referred to as "Coats"). Claims 9-11 and 14-19 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Ichikawa in view of Carver. Claims 5-6 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Ichikawa in view of Coats and Heminger et al. Claim 7 stands rejected under 35 U.S.C § 103(a) as being unpatentable over Ichikawa in view of Coats and Ohura et al. Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ichikawa in view of Carver and Heminger, and claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ichikawa in view of Carver and Ohura.

By this amendment, the applicant has amended the claims to more particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

The Examiner has cited the Ichikawa and Coats references to reject claim 1 as obvious.

Claim 1 has been amended to recite that the sensing circuit senses the rate of change of voltage with respect to time at a first main electrode of the power switching transistor coupled to a storage capacitor whereby the rate of change of voltage at the first main electrode is proportional to the magnitude of the current flowing through the first main electrode. Although Ichikawa teaches monitoring the dv/dt across a power switching transistor to be protected (see Fig. 23), Ichikawa neither teaches nor suggests that the dv/dt is proportional to the magnitude of the current flowing through the power switching transistor.

Ichikawa shows a dv/dt detecting circuit in Fig. 23. However, that circuit must be connected across the power transistor to detect dv/dt. There is no suggestion in Ichikawa of providing a dv/dt detecting circuit as in the present invention which is coupled to a switching transistor main electrode (coupled to a storage capacitor) thereby to detect the magnitude of the current flowing through the switching transistor main terminal. Where Ichikawa does show a current sensing circuit (Fig. 21), he uses a current sensor 15 (like a series resistor or current transformer). He teaches and suggests nothing concerning the novel circuit of the invention that uses the combination of a storage capacitor coupled to the main terminal and the sensing circuit claimed that detects the dv/dt across the storage capacitor that is proportional to the current magnitude flowing in the power switch thereby to protect the power switch from excessive current.

The Examiner has cited Coats for teaching removing a control signal to the control electrode of a power switching transistor to turn off the power switching transistor if overcurrent is present. The Coats reference does not teach or suggest sensing the rate of change of voltage with respect to time at a first main electrode of a power switching transistor coupled to a storage capacitor wherein the rate of change of voltage is proportional to the magnitude of the current flowing through the first main electrode. There is nothing in the Ichikawa and Coats references, taken alone or in combination, which suggests the invention as now more distinctly claimed. Even when this combination is made, the result is not the invention because Ichikawa requires a dv/dt detecting circuit that directly monitors dv/dt across the switch in contrast to the invention.

Although the Examiner did not cite Carver in rejecting Claim 1, Carver also fails to supply teaching missing from Ichikawa. Carver teaches an amplifier with protective energy limiter circuit components. However, Carver does not teach or suggest a sensing circuit that senses the rate of change of voltage with respect to time at a first main electrode of the power switching transistor wherein the rate of change of voltage is proportional to the magnitude of the current flowing through the first main electrode as now recited in claim 1.

Accordingly, the applicant believes claim 1 as amended is allowable over the art of record. Because claims 2-8 depend from claim 1, they are also believed to be allowable over the art of record.

The Examiner has cited the Ichikawa and Carver references to reject claim 9 as obvious.

As an initial matter, the applicant respectfully disagrees with the Examiner's interpretation of the operation of the circuit of Carver. Referring to the energy limiter circuit of Carver, (shown in Figure 2), the Examiner called the capacitor C1 a sensing capacitor, the capacitor C5 a storage capacitor, and the resistor R6 a sensing resistor. The applicant respectfully calls the Examiner's attention to the Carver reference at column 4, lines 1-27 wherein the capacitor C1 is described as an integrating capacitor. The resistor R7 (not labeled in Fig 2, but the resistor coupled between C1 and R9) and the capacitor C1 form the time integral of the current Idt. Capacitor C1 of Carver does not function in the same manner as the sensing capacitor C8 of the present invention which is adapted to generate a current representative of the rate of change of voltage with respect to time across the storage capacitor. Further, resistor R6 is coupled in series with capacitor C1, not as claimed between a reference potential and the control

electrode and second terminal of the sensing capacitor. It simply does not function in the same way as the claimed sensing resistor.

Claim 9 has been amended to more particularly point out and distinctly claim an overcurrent protection circuit for a power switching transistor wherein the power switching transistor has a control electrode and first and second main electrodes, the first main electrode coupled to a storage capacitor, the circuit comprising a protection transistor having a control electrode and first and second main electrodes, the first main electrode of the protection transistor coupled to the control electrode of the power switching transistor and the second main electrode of the protection transistor coupled to a reference potential; a sensing capacitor having first and second terminals, the first terminal of the sensing capacitor coupled to the first main electrode of the power switching transistor and the storage capacitor, the sensing capacitor being adapted to generate a current representative of the rate of change of voltage with respect to time across the storage capacitor; and a sensing resistor having first and second terminals, the first terminal of the sensing resistor coupled to the reference potential, and the second terminal of the sensing resistor coupled to both the control electrode of the protection transistor and the second terminal of the sensing capacitor, the sensing capacitor providing a current to the sensing resistor to develop a sensing voltage across the sensing resistor to turn on the protection transistor if the sensing voltage across the sensing resistor exceeds a predefined sensing voltage value; wherein the protection transistor is adapted to remove a control signal to the control electrode of the power switching transistor to turn off the power switching transistor if the rate of change of voltage with respect to time across the storage capacitor exceeds a first predefined rate of change value.

Neither Ichikawa nor Carver teaches or suggests an overcurrent protection circuit with the structure and interrelationship of elements as now described in Claim 9. Accordingly, the applicant believes independent claim 9 as amended is allowable over the art of record. Claim 10 has been canceled, and claims 11 and 13 have been amended to depend from claim 9. Because claims 11-14 depend from claim 9, they are also believed to be allowable over the art of record.

Carver, at column 4, lines 28 to 45 describes resistor R4 and capacitor C5 as developing a voltage which appears at the wiring summing junction A and is the time derivative, dv/dt, of the output voltage. However, the Examiner should note that this is a different circuit than the circuit

claimed. The amplifier output is coupled to the wiring junction (base of Q9) by numerous other resistors and capacitors. Resistor R4 is connected in series with C5, not as claimed. Further, the switch Q9 has its emitter not connected to the reference potential ground, but instead to the amplifier output.

Again, the Examiner cited to the Ichikawa and Carver references to reject claim 15 as obvious.

Independent claim 15 has also been amended in a manner similar to claim 9, and claims 16-19 have been canceled. The applicant submits, for the same reasons, that neither the Ichikawa nor the Carver reference teaches or suggests the invention as now claimed; and the applicant believes claim 15 as amended is allowable over the art of record.

The present invention is developed from the inventive insight that the current through the power switching transistor feeding a storage capacitor can be indirectly measured by detecting the time rate of change of voltage across the storage capacitor. This is proportional to the current into the capacitor and thus the current through the switching transistor.

The present invention provides an elegantly simple way to monitor the current to protect the switch without resorting to the well known but inefficient or expensive methods of the prior art, as shown for example by Ichikawa, Fig. 21, where a series current sensing resistor (inefficient) or current transformer (expensive) is used for this purpose. The present invention avoids these methods entirely with a novel, unobvious approach. The Examiner is requested to reconsider the rejections of the claims. An earnest attempt has been made to distinguish the prior art and to explain the novelty and unobviousness of the invention over the prior art.

Accordingly, the applicant submits that all claims in this application are now in condition for allowance, prompt notification of which is respectfully requested.

Respectfully submitted,

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